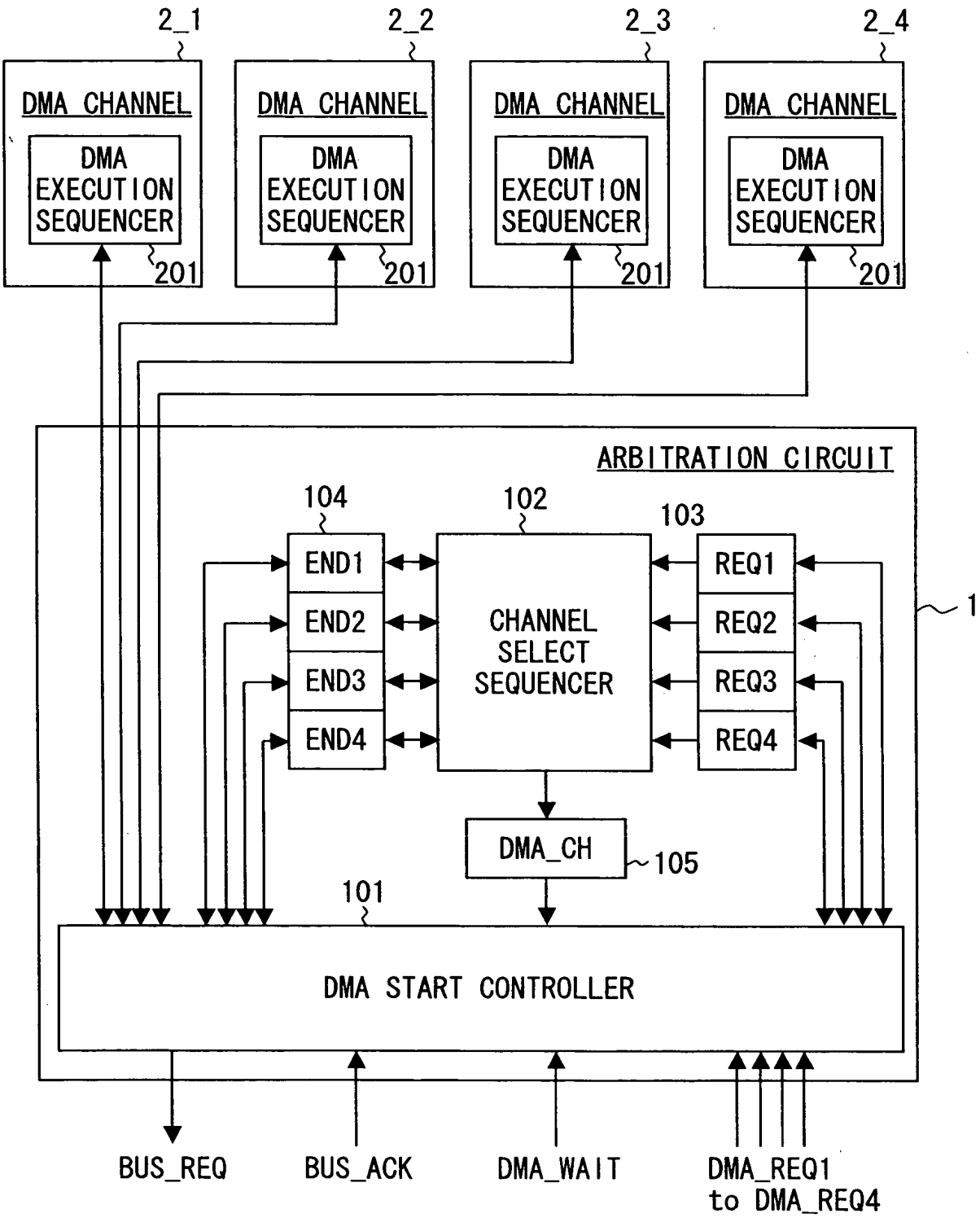
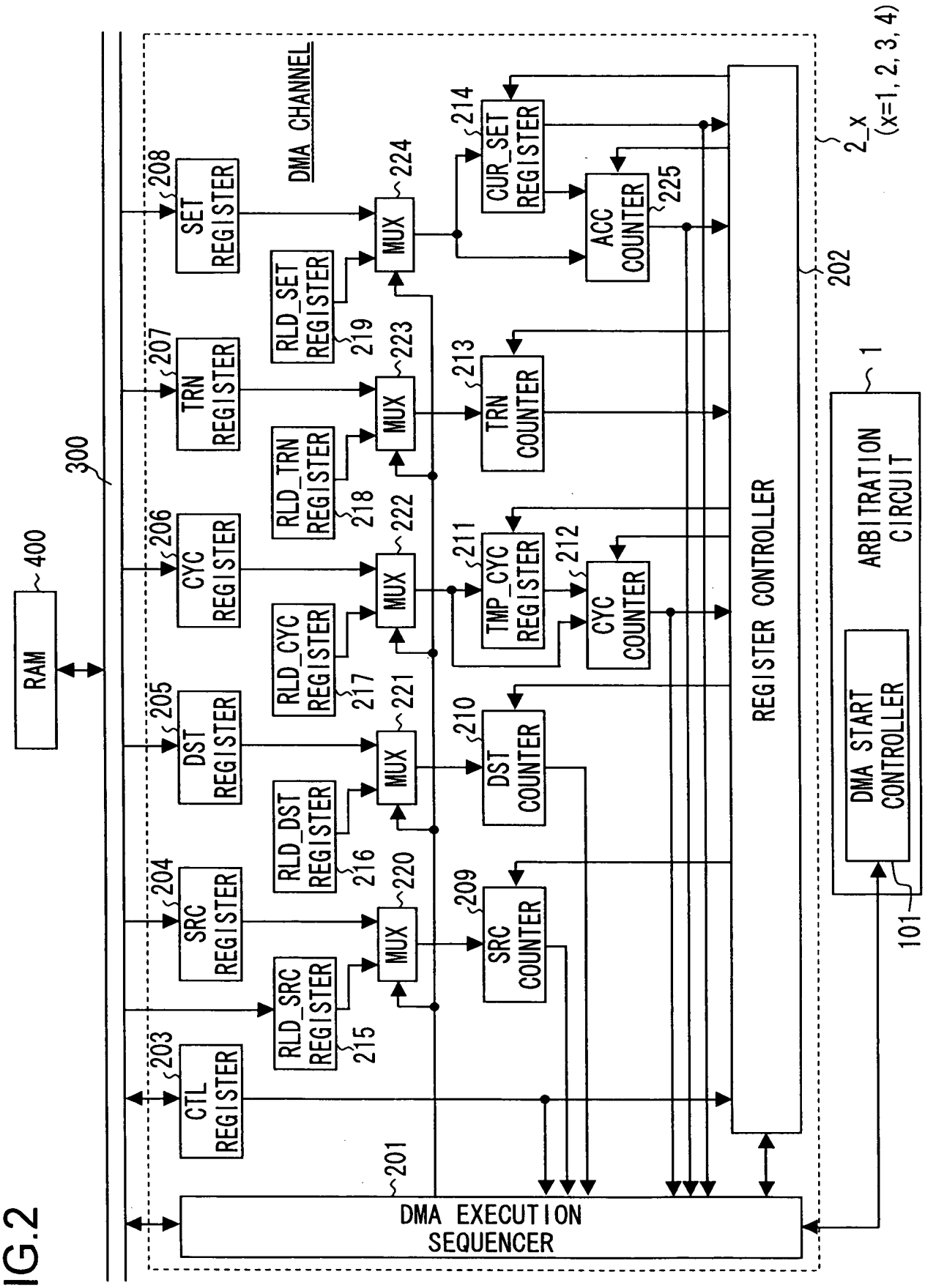
Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
Appln. No. : Unknown
Docket No.: 103213-00057

FIG.1



Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
Appln. No. : Unknown
Docket No.: 103213-00057

FIG.2



Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
Appln. No. : Unknown
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FIG.3

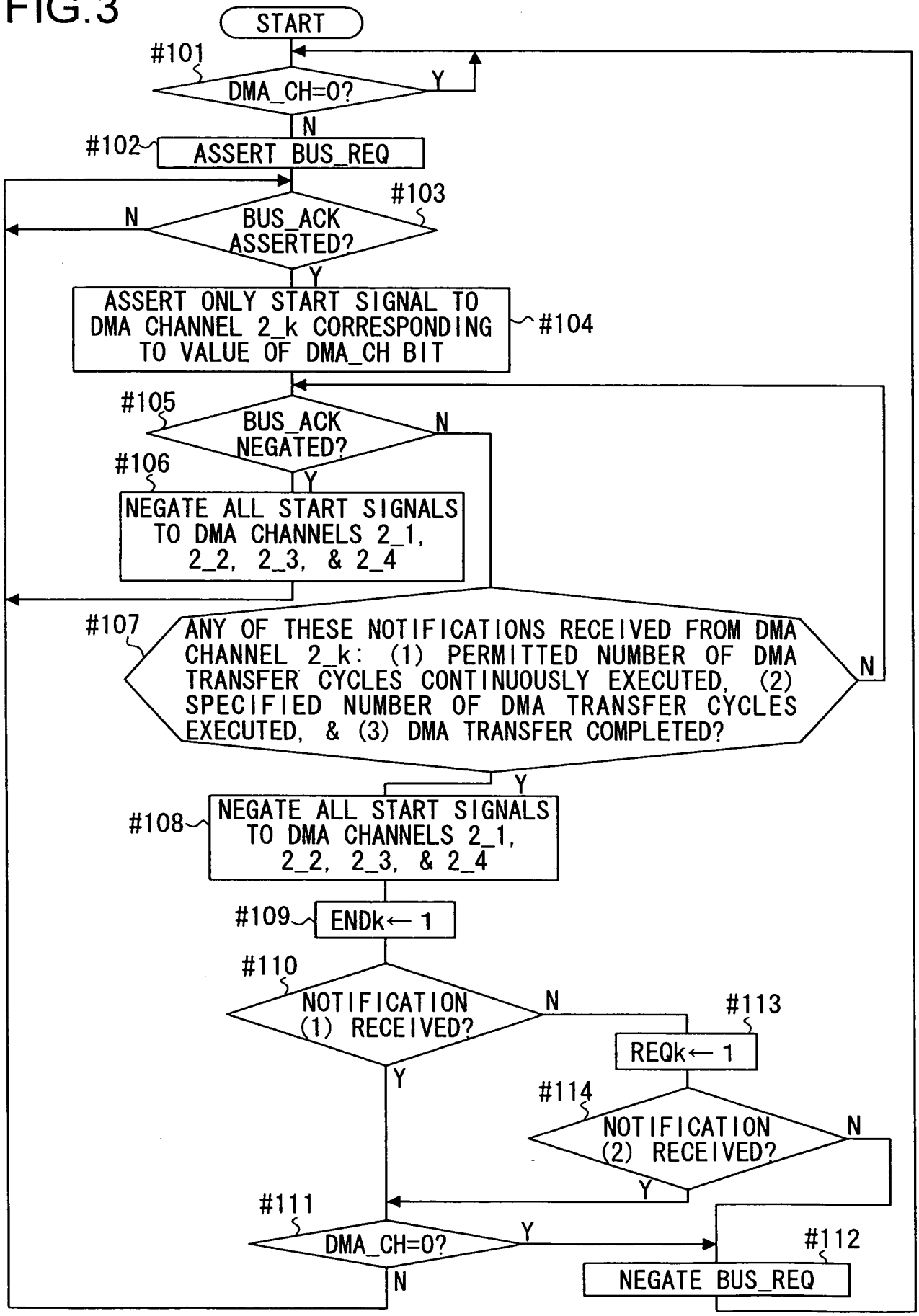

FIG.4

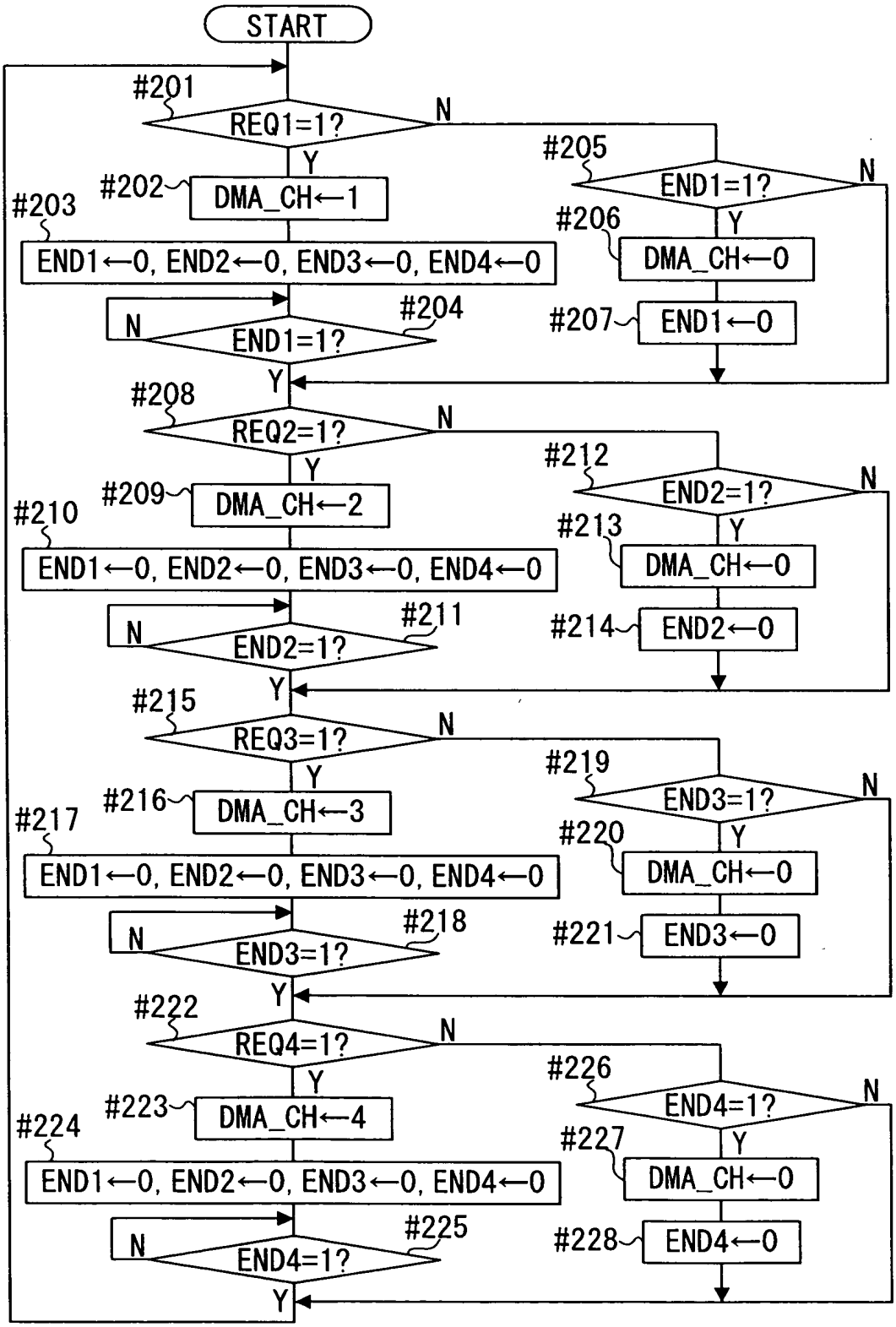
START
#201
REQ1=1?
N
Y
#202
DMA_CH←1
#203
END1←0, END2←0, END3←0, END4←0
#204
N
END1=1?
Y
#205
END1=1?
N
Y
#206
DMA_CH←0
#207
END1←0
#208
REQ2=1?
N
Y
#209
DMA_CH←2
#210
END1←0, END2←0, END3←0, END4←0
#211
N
END2=1?
Y
#212
END2=1?
N
Y
#213
DMA_CH←0
#214
END2←0
#215
REQ3=1?
N
Y
#216
DMA_CH←3
#217
END1←0, END2←0, END3←0, END4←0
#218
N
END3=1?
Y
#219
END3=1?
N
Y
#220
DMA_CH←0
#221
END3←0
#222
REQ4=1?
N
Y
#223
DMA_CH←4
#224
END1←0, END2←0, END3←0, END4←0
#225
N
END4=1?
Y
#226
END4=1?
N
Y
#227
DMA_CH←0
#228
END4←0

FIG.5

ADDRESS(Hex)	CONTENTS OF DATA
⋮	⋮
20000000-20000003	START ADDRESS(20007774) IN RAM 400 WHERE INFORMATION NEEDED FOR 2ND DMA TRANSFER SESSION IS STORED
20000004-20000007	INFORMATION INDICATING START ADDRESS OF SOURCE IN 1ST DMA TRANSFER SESSION
20000008-2000000B	INFORMATION INDICATING START ADDRESS OF DESTINATION IN 1ST DMA TRANSFER SESSION
2000000C-2000000D	INFORMATION INDICATING NUMBER OF CYCLES INVOLVED IN ONE DMA TRANSFER SESSION IN 1ST DMA TRANSFER SESSION
2000000E-2000000F	INFORMATION INDICATING NUMBER OF DMA TRANSFER SESSIONS TO BE EXECUTED IN 1ST DMA TRANSFER SESSION
20000010-20000011	OTHER INFORMATION RELATING TO 1ST DMA TRANSFER SESSION
20000012	CONTROL INFORMATION RELATING TO 1ST DMA TRANSFER SESSION S/W_START = 0 MOD[1,0] = [1,1]
⋮	⋮
20007774-20007777	START ADDRESS(ARBITRARY) IN RAM 400 WHERE INFORMATION NEEDED FOR 3RD DMA TRANSFER SESSION IS STORED
20007778-2000777B	INFORMATION INDICATING START ADDRESS OF SOURCE IN 2ND DMA TRANSFER SESSION
2000777C-2000777F	INFORMATION INDICATING START ADDRESS OF DESTINATION IN 2ND DMA TRANSFER SESSION
20007780-20007781	INFORMATION INDICATING NUMBER OF CYCLES INVOLVED IN ONE DMA TRANSFER SESSION IN 2ND DMA TRANSFER SESSION
20007782-20007783	INFORMATION INDICATING NUMBER OF DMA TRANSFER SESSIONS TO BE EXECUTED IN 2ND DMA TRANSFER SESSION
20007784-20007785	OTHER INFORMATION RELATING TO 2ND DMA TRANSFER SESSION
20007786	CONTROL INFORMATION RELATING TO 2ND DMA TRANSFER SESSION S/W_START = 0 MOD[1,0] = [1,0]
⋮	⋮

Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
Appln. No. : Unknown
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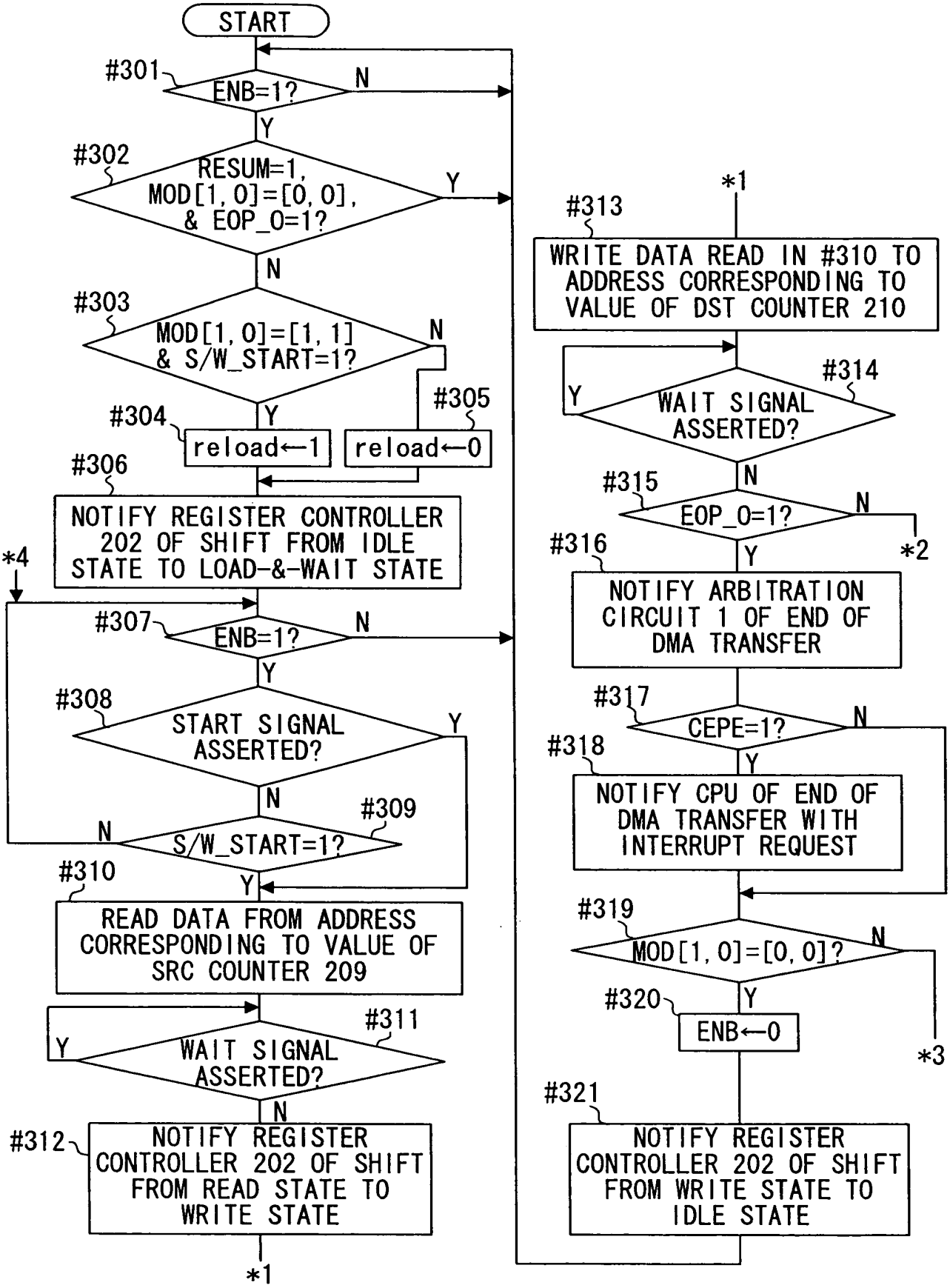
FIG.6



Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
Appln. No. : Unknown
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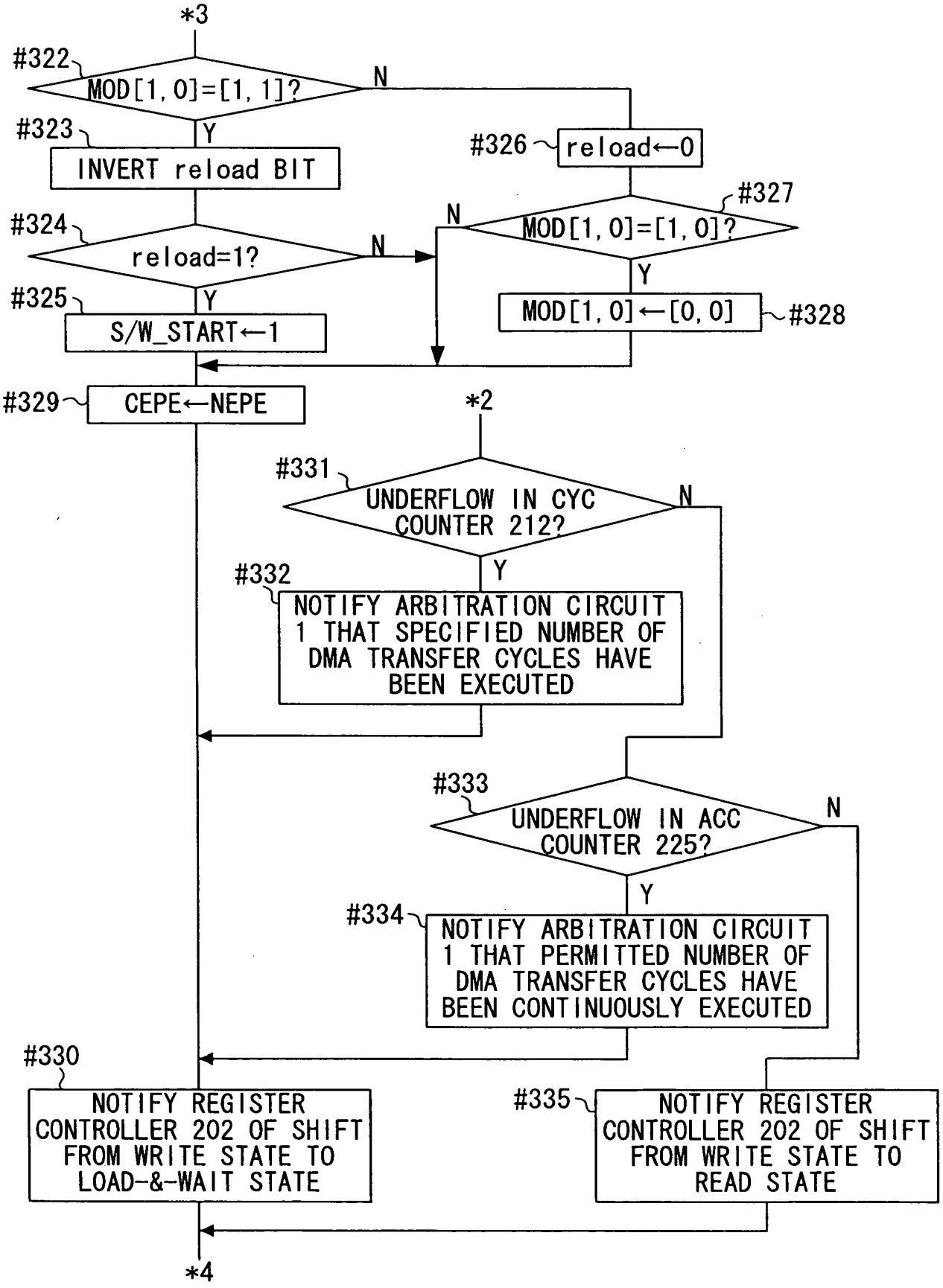
FIG.7



Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
Appln. No. : Unknown
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FIG.8

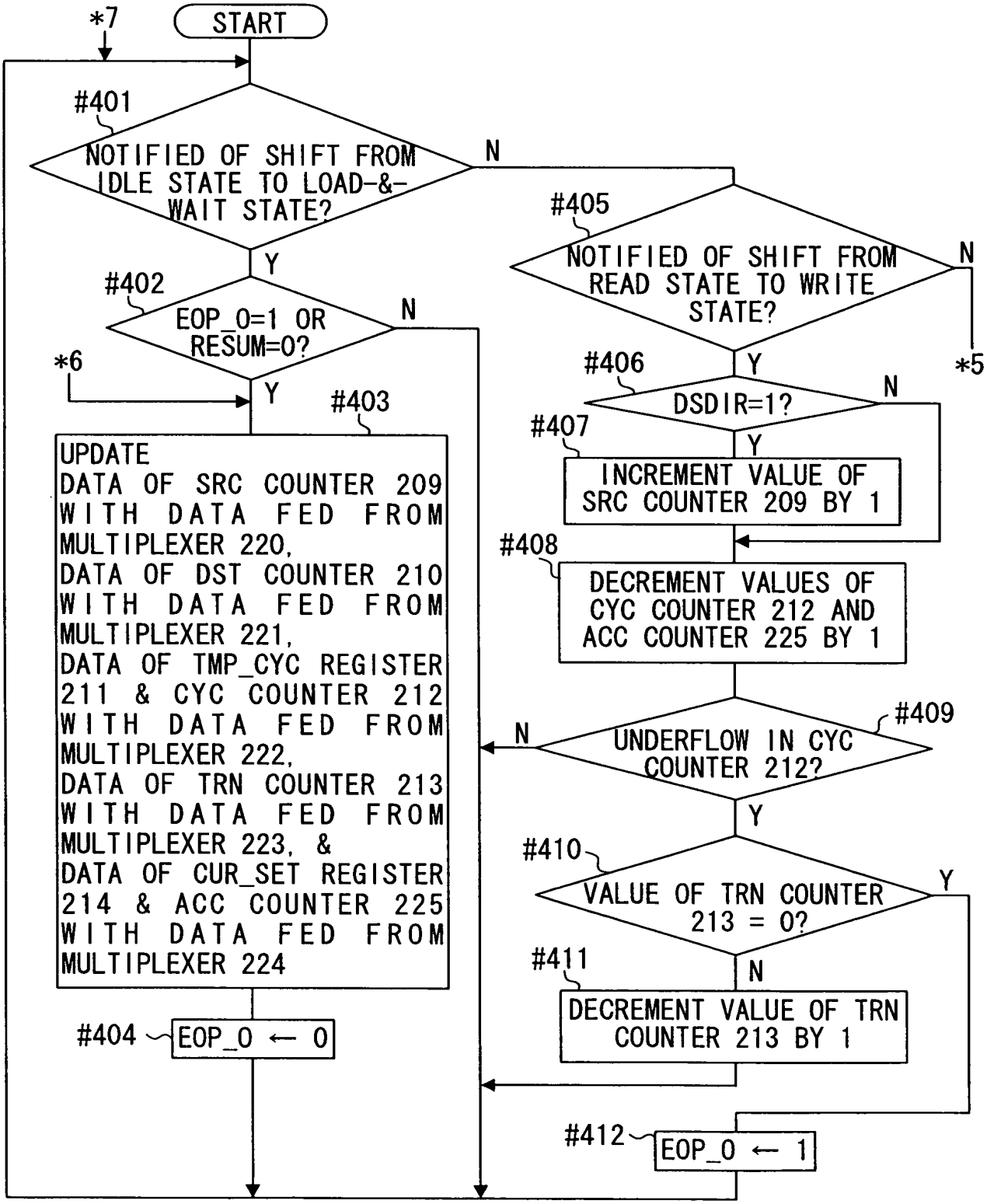


FIG.9

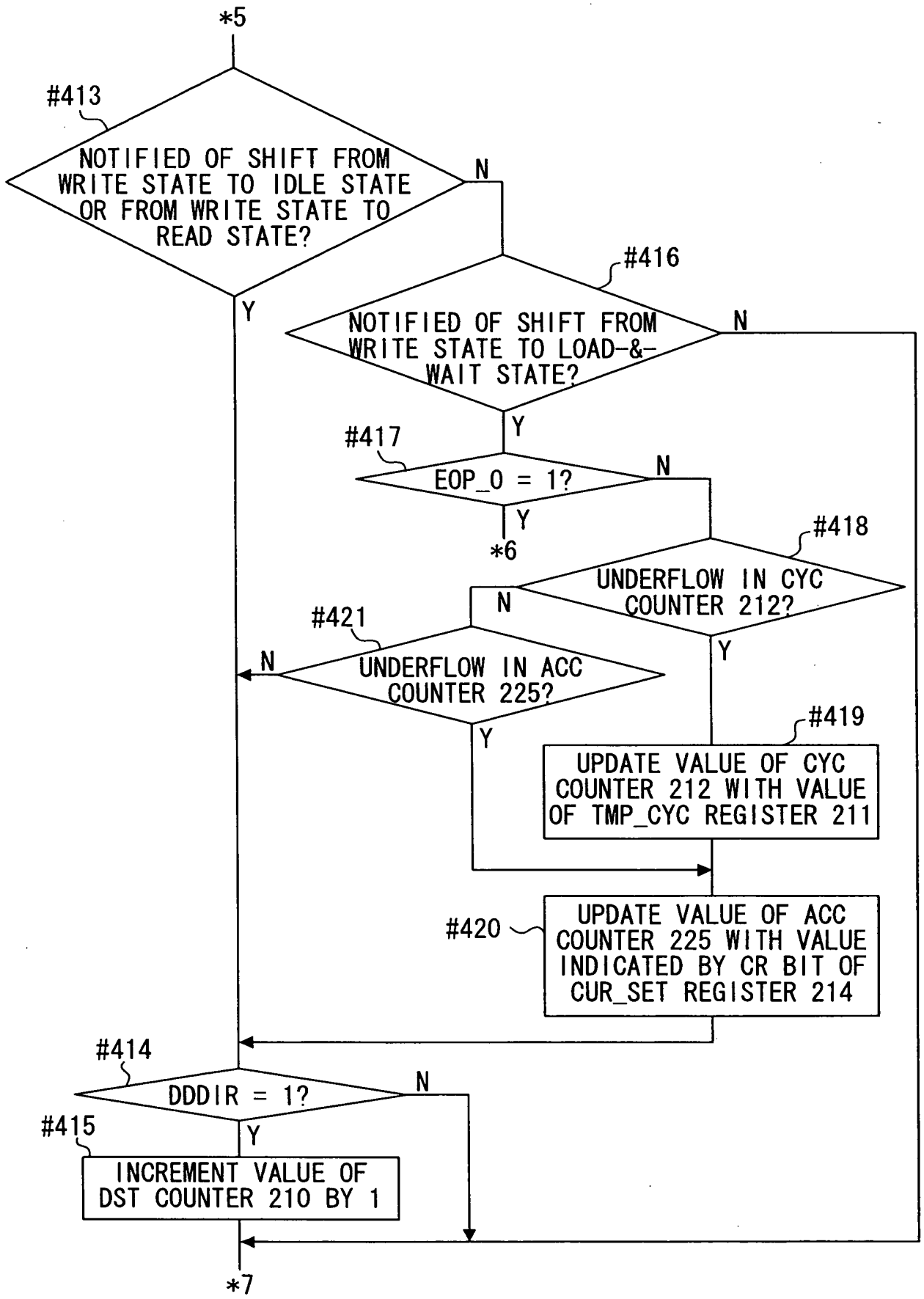

*5
#413
NOTIFIED OF SHIFT FROM WRITE STATE TO IDLE STATE OR FROM WRITE STATE TO READ STATE?
N
Y
#416
NOTIFIED OF SHIFT FROM WRITE STATE TO LOAD-&-WAIT STATE?
N
Y
#417
EOP_0 = 1?
N
Y
*6
#418
UNDERFLOW IN CYC COUNTER 212?
N
Y
#421
UNDERFLOW IN ACC COUNTER 225?
N
Y
#419
UPDATE VALUE OF CYC COUNTER 212 WITH VALUE OF TMP_CYC REGISTER 211
#420
UPDATE VALUE OF ACC COUNTER 225 WITH VALUE INDICATED BY CR BIT OF CUR_SET REGISTER 214
#414
DDDIR = 1?
N
Y
#415
INCREMENT VALUE OF DST COUNTER 210 BY 1
*7

FIG.10

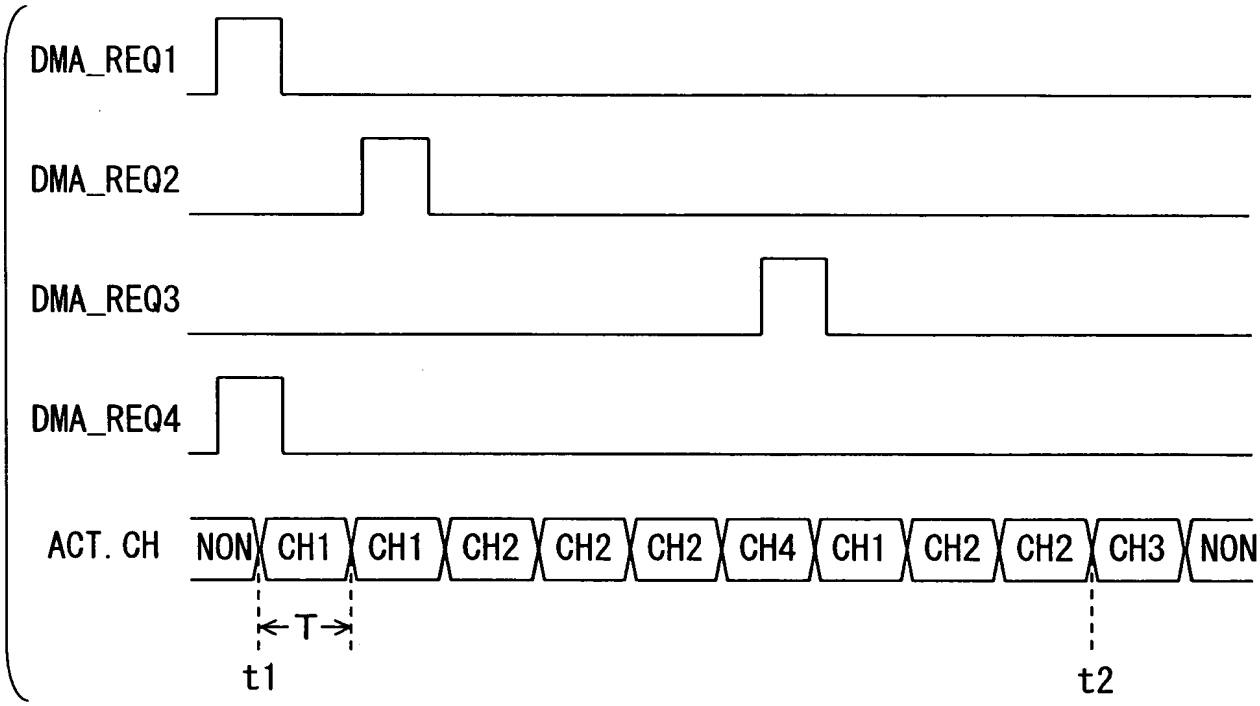


FIG.11A PRIOR ART

PRIORITY	CHANNEL
1	CH2
2	CH3
3	CH4
4	CH1

FIG.11B PRIOR ART

PRIORITY	CHANNEL
1	CH3
2	CH4
3	CH1
4	CH2

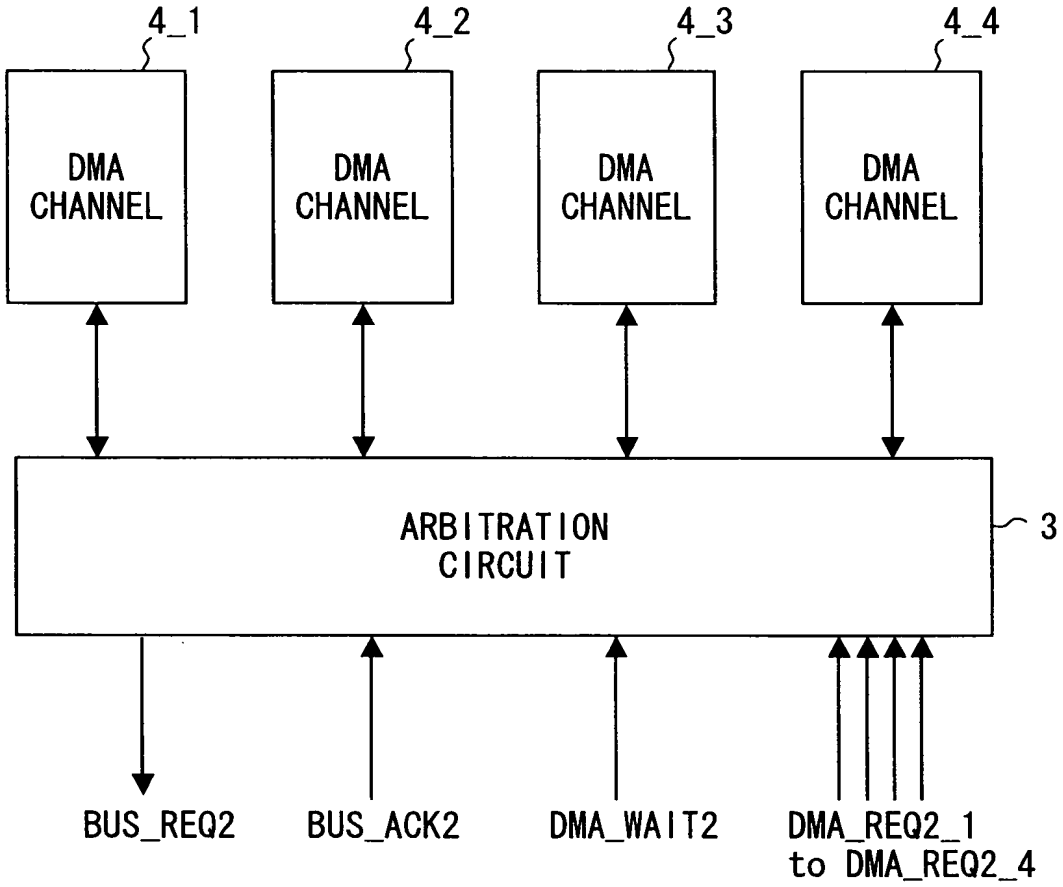
FIG.11C PRIOR ART

PRIORITY	CHANNEL
1	CH4
2	CH1
3	CH2
4	CH3

FIG.11D PRIOR ART

PRIORITY	CHANNEL
1	CH1
2	CH2
3	CH3
4	CH4

FIG.12


4_1
4_2
4_3
4_4
DMA CHANNEL
DMA CHANNEL
DMA CHANNEL
DMA CHANNEL
ARBITRATION CIRCUIT
3
BUS_REQ2
BUS_ACK2
DMA_WAIT2
DMA_REQ2_1 to DMA_REQ2_4

Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
Appln. No. : Unknown
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FIG.13

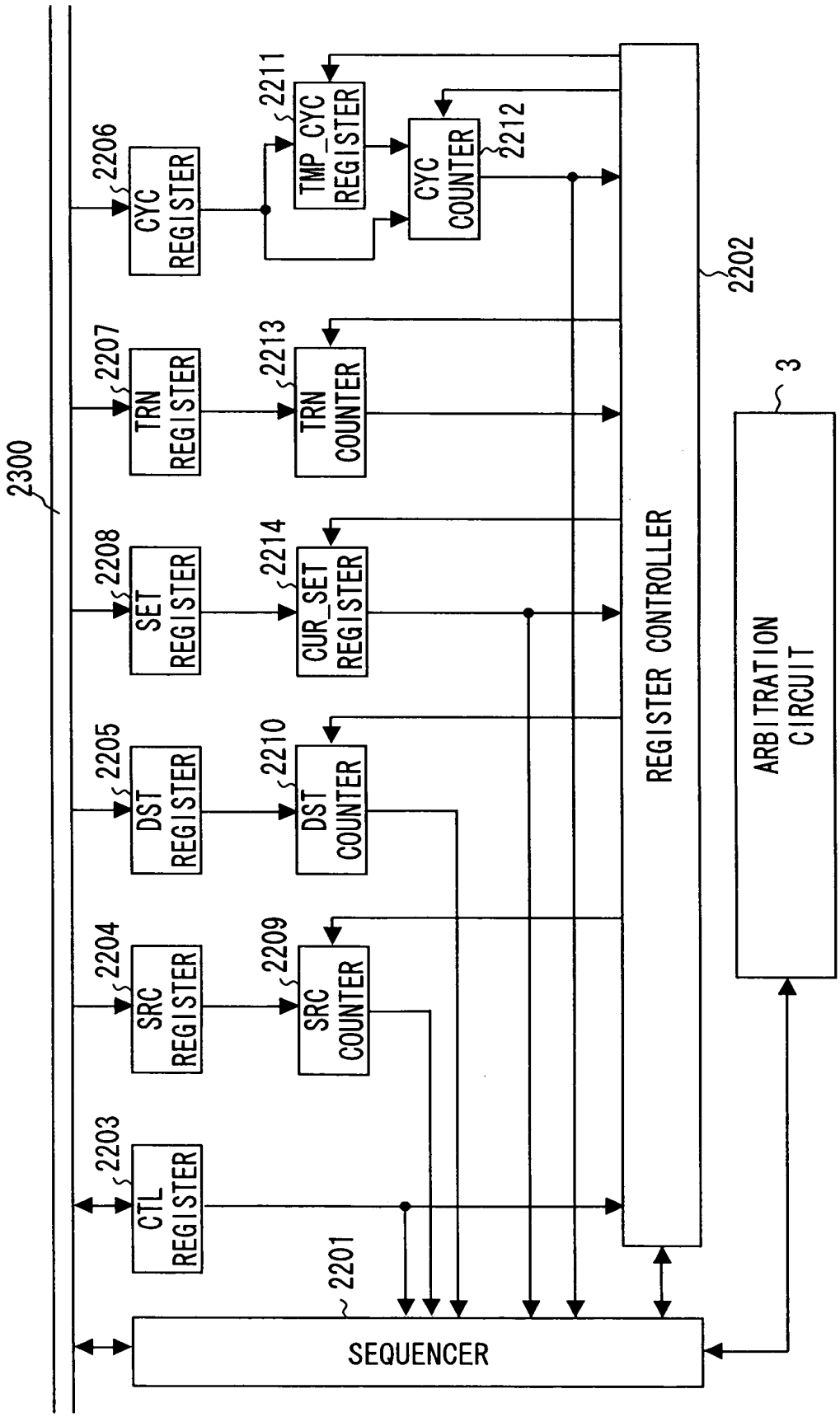


FIG.14

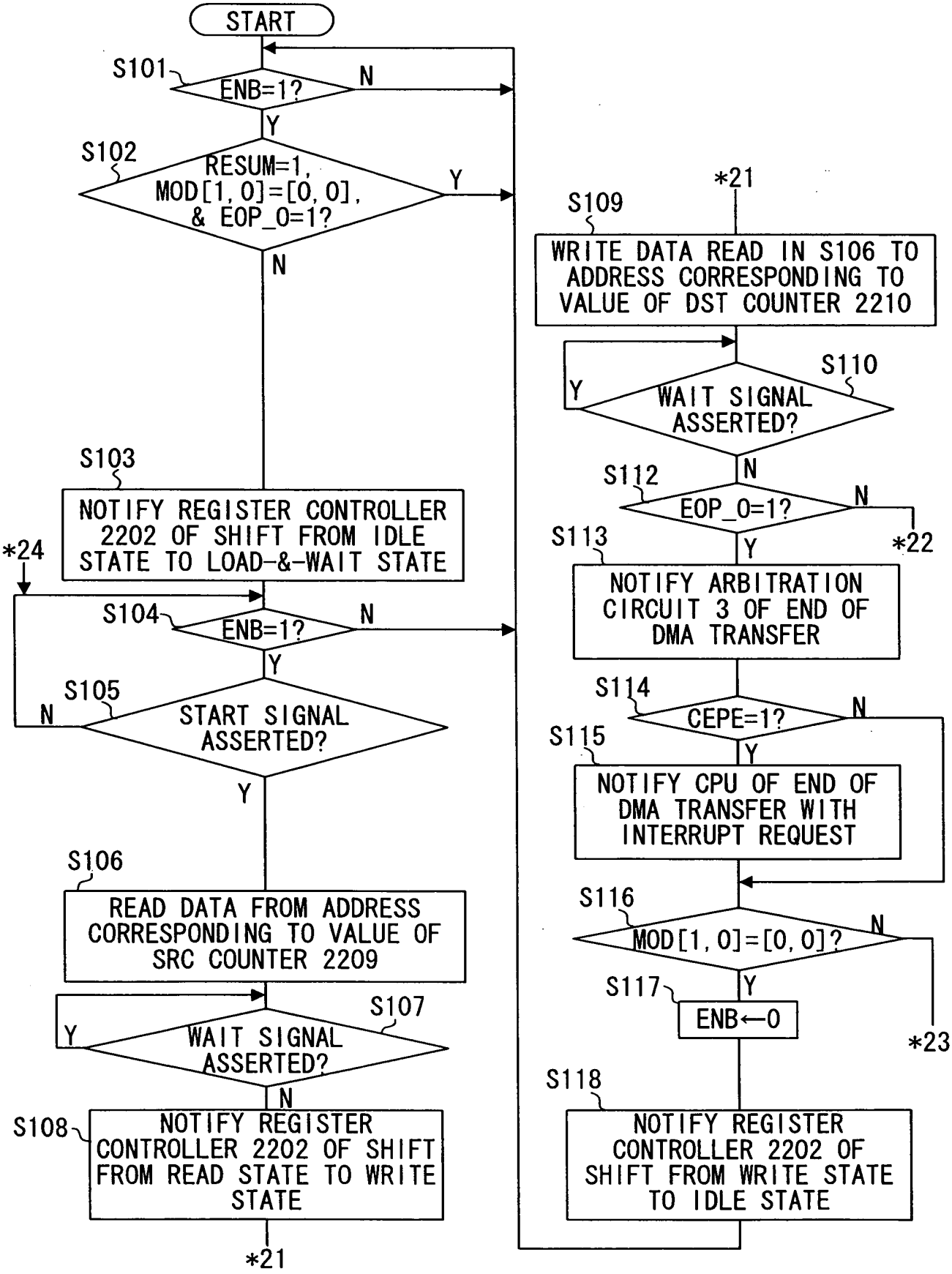
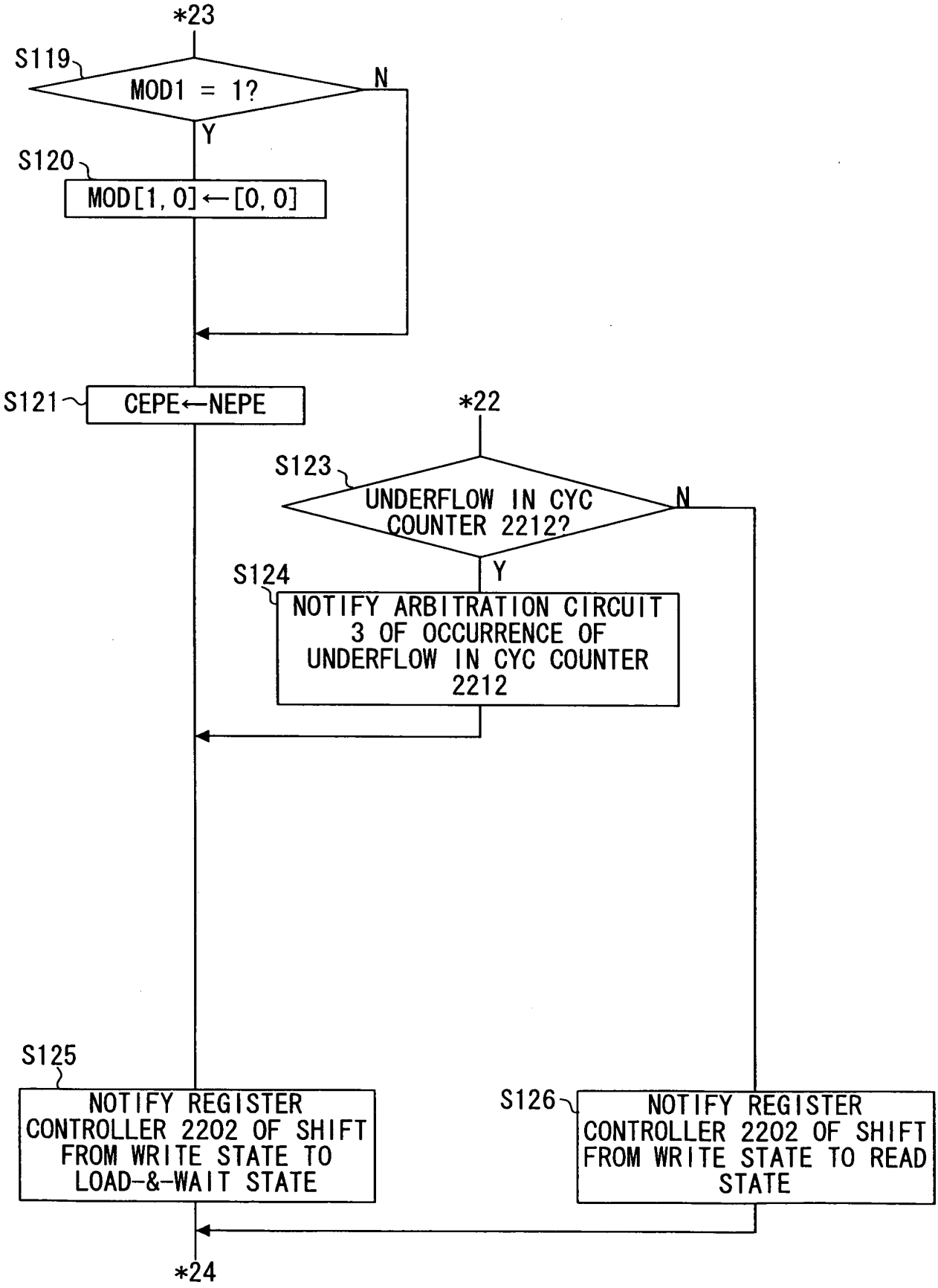

START
S101
ENB=1?
N
Y
S102
RESUM=1, MOD[1,0]=[0,0], & EOP_0=1?
Y
N
S103
NOTIFY REGISTER CONTROLLER 2202 OF SHIFT FROM IDLE STATE TO LOAD-&-WAIT STATE
*24
S104
ENB=1?
N
Y
S105
START SIGNAL ASSERTED?
N
Y
S106
READ DATA FROM ADDRESS CORRESPONDING TO VALUE OF SRC COUNTER 2209
S107
WAIT SIGNAL ASSERTED?
Y
N
S108
NOTIFY REGISTER CONTROLLER 2202 OF SHIFT FROM READ STATE TO WRITE STATE
*21
*21
S109
WRITE DATA READ IN S106 TO ADDRESS CORRESPONDING TO VALUE OF DST COUNTER 2210
S110
WAIT SIGNAL ASSERTED?
Y
N
S112
EOP_0=1?
N
*22
Y
S113
NOTIFY ARBITRATION CIRCUIT 3 OF END OF DMA TRANSFER
S114
CEPE=1?
N
Y
S115
NOTIFY CPU OF END OF DMA TRANSFER WITH INTERRUPT REQUEST
S116
MOD[1,0]=[0,0]?
N
Y
S117
ENB←0
*23
S118
NOTIFY REGISTER CONTROLLER 2202 OF SHIFT FROM WRITE STATE TO IDLE STATE

FIG.15


*23
S119
MOD1 = 1?
N
Y
S120
MOD[1, 0]←[0, 0]
S121
CEPE←NEPE
*22
S123
UNDERFLOW IN CYC COUNTER 2212?
N
Y
S124
NOTIFY ARBITRATION CIRCUIT 3 OF OCCURRENCE OF UNDERFLOW IN CYC COUNTER 2212
S125
NOTIFY REGISTER CONTROLLER 2202 OF SHIFT FROM WRITE STATE TO LOAD-&-WAIT STATE
S126
NOTIFY REGISTER CONTROLLER 2202 OF SHIFT FROM WRITE STATE TO READ STATE
*24

Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
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FIG.16

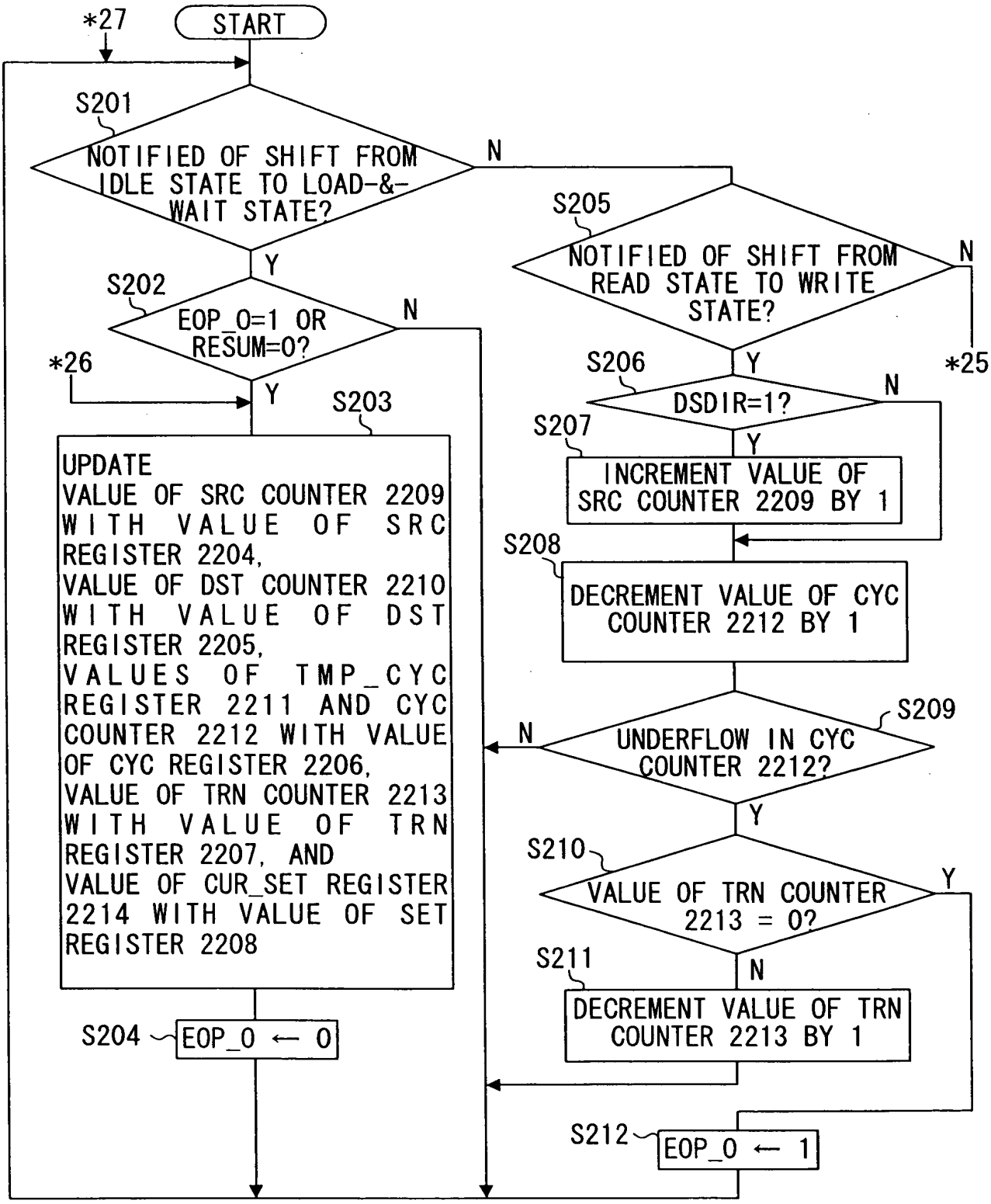
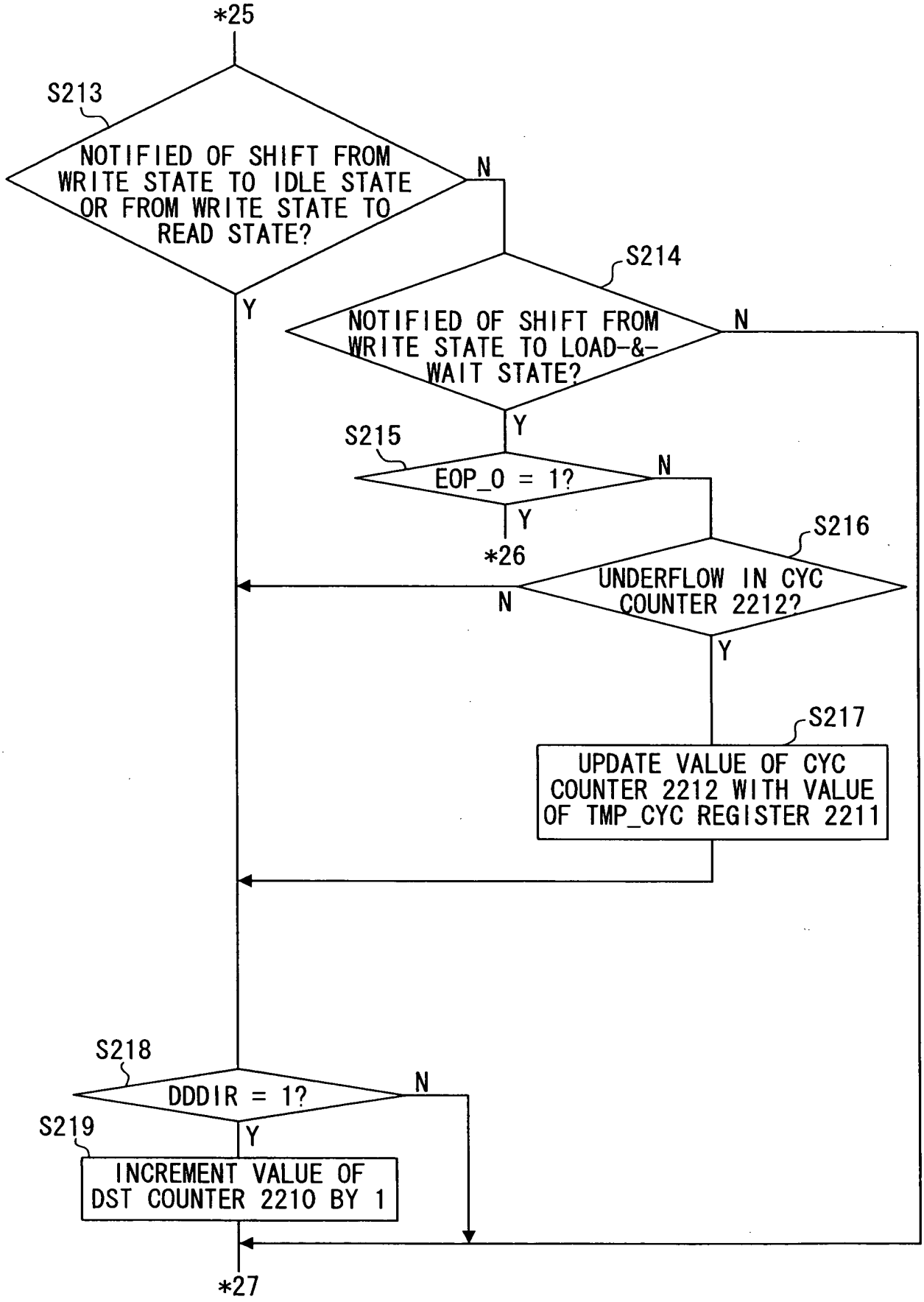


FIG.17


*25
S213
NOTIFIED OF SHIFT FROM WRITE STATE TO IDLE STATE OR FROM WRITE STATE TO READ STATE?
N
Y
S214
NOTIFIED OF SHIFT FROM WRITE STATE TO LOAD-&-WAIT STATE?
N
Y
S215
EOP_0 = 1?
N
Y
*26
S216
UNDERFLOW IN CYC COUNTER 2212?
N
Y
S217
UPDATE VALUE OF CYC COUNTER 2212 WITH VALUE OF TMP_CYC REGISTER 2211
S218
DDDIR = 1?
N
Y
S219
INCREMENT VALUE OF DST COUNTER 2210 BY 1
*27

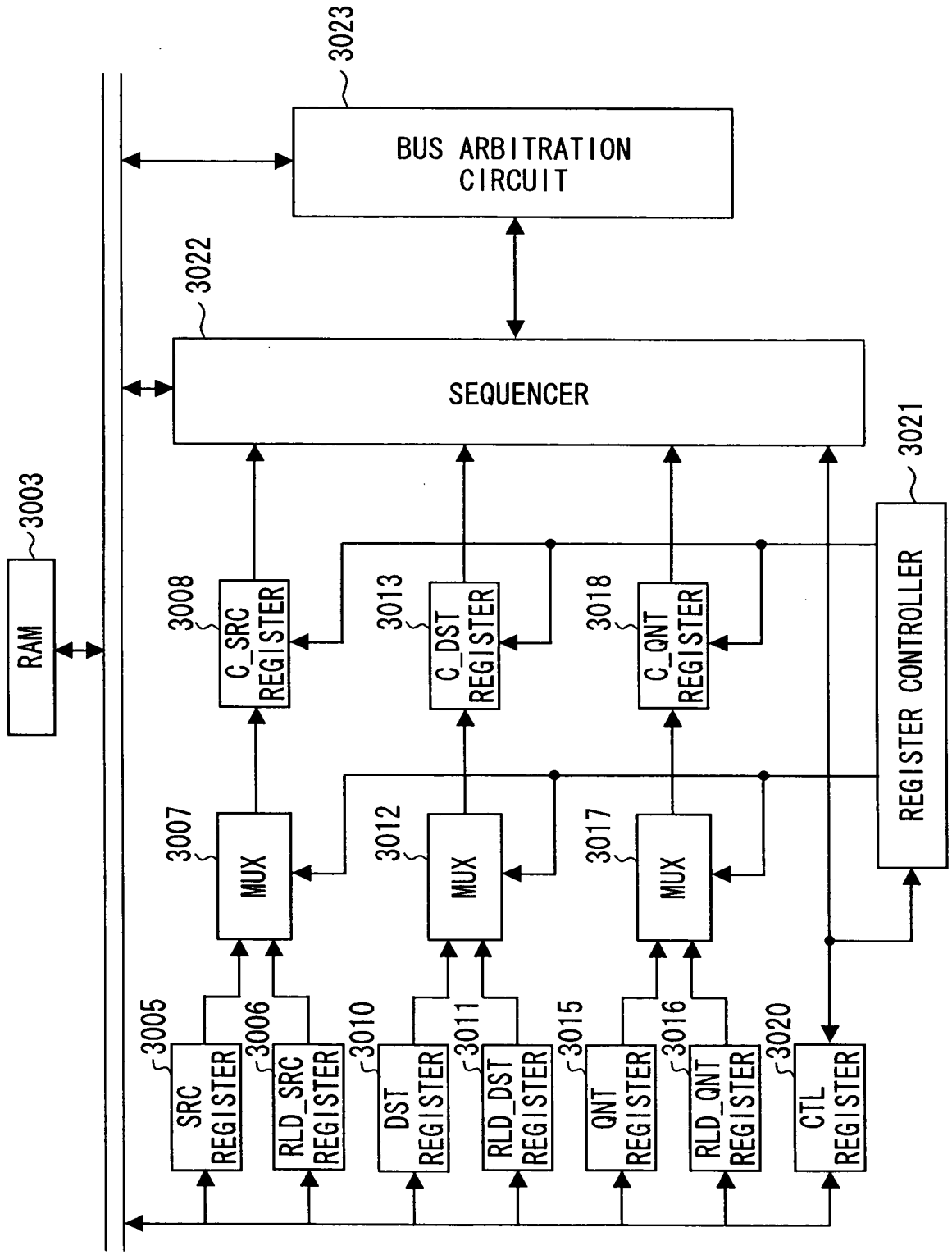

3023
BUS ARBITRATION CIRCUIT
3022
SEQUENCER
3021
REGISTER CONTROLLER
3003
RAM
3008
C_SRC REGISTER
3013
C_DST REGISTER
3018
C_QNT REGISTER
3007
MUX
3012
MUX
3017
MUX
3005
SRC REGISTER
3006
RLD_SRC REGISTER
3010
DST REGISTER
3011
RLD_DST REGISTER
3015
QNT REGISTER
3016
RLD_QNT REGISTER
3020
CTL REGISTER

FIG.18

FIG.19

ADDRESS (Hex)	VALUE
1000	2000 (Hex)
1001	SA1
1002	DA1
1003	BYTE1
1004	ENB BIT=1, RLD_ENB BIT=1
.	.
.	.
.	.
2000	ARBITRARY
2001	SA2
2002	DA2
2003	BYTE2
2004	ENB BIT=1, RLD_ENB BIT=0

FIG.20

ENB BIT	RLD_ENB BIT	PREVIOUS OPERATION	REGISTERS SELECTED BY MULTIPLEXERS 7, 12, &17	OPERATION
0	ARBITRARY	ARBITRARY	ARBITRARY	NO OPERATION
1	0	ARBITRARY	SRC REGISTER 3005 DST REGISTER 3010 QNT REGISTER 3015	NORMAL DMA TRANSFER
1	1	NORMAL DMA TRANSFER	RLD_SRC REGISTER 3006 RLD_DST REGISTER 3011 RLD_QNT REGISTER 3016	RELOAD
		RELOAD	SRC REGISTER 3005 DST REGISTER 3010 QNT REGISTER 3015	NORMAL DMA TRANSFER

FIG.21

	(1)	(2)	(3)
SRC REGISTER 3005	ARBITRARY	SA1	SA2
RLD_SRC REGISTER 3006	1000(Hex)	2000(Hex)	ARBITRARY
DST REGISTER 3010	ARBITRARY	DA1	DA2
RLD_DST REGISTER 3011	ADDRESS OF RLD_SRC REGISTER 3006	←	←
QNT REGISTER 3015	ARBITRARY	BYTE1	BYTE2
RLD_QNT REGISTER 3016	5	←	←
CTL REGISTER 3020	ENB BIT=1 RLD_ENB BIT=1	ENB BIT=1 RLD_ENB BIT=1	ENB BIT=1 RLD_ENB BIT=0

Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
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Appln. No.: Unknown
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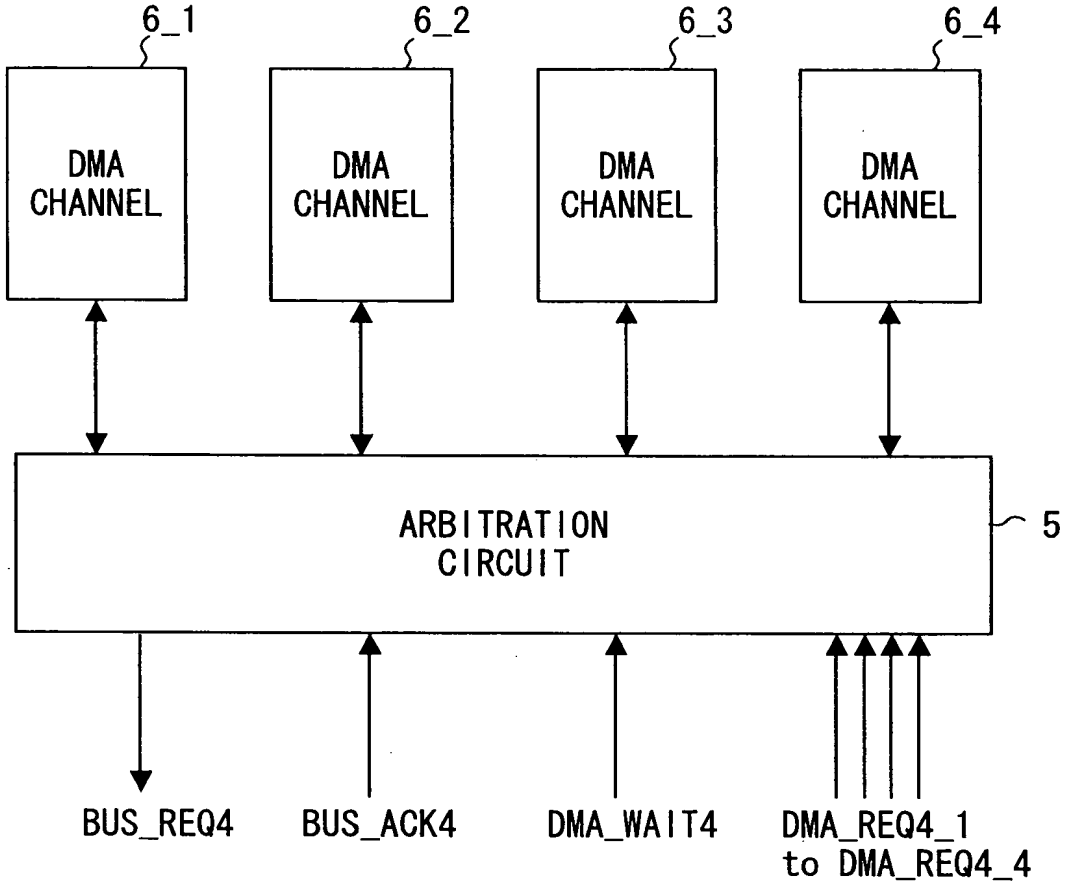
FIG.22


6_1
6_2
6_3
6_4
DMA CHANNEL
DMA CHANNEL
DMA CHANNEL
DMA CHANNEL
ARBITRATION CIRCUIT
5
BUS_REQ4
BUS_ACK4
DMA_WAIT4
DMA_REQ4_1 to DMA_REQ4_4

Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
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FIG.23

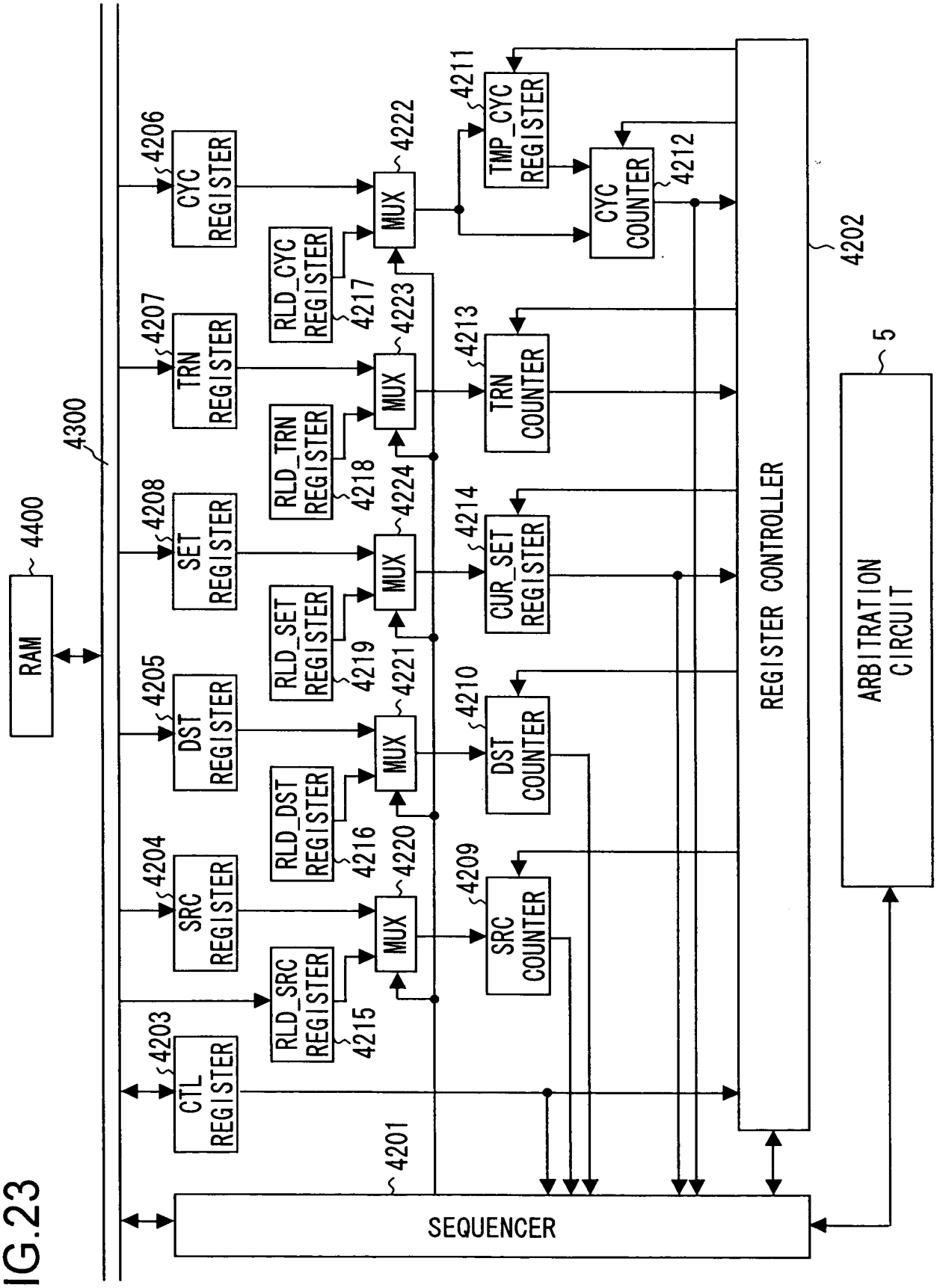
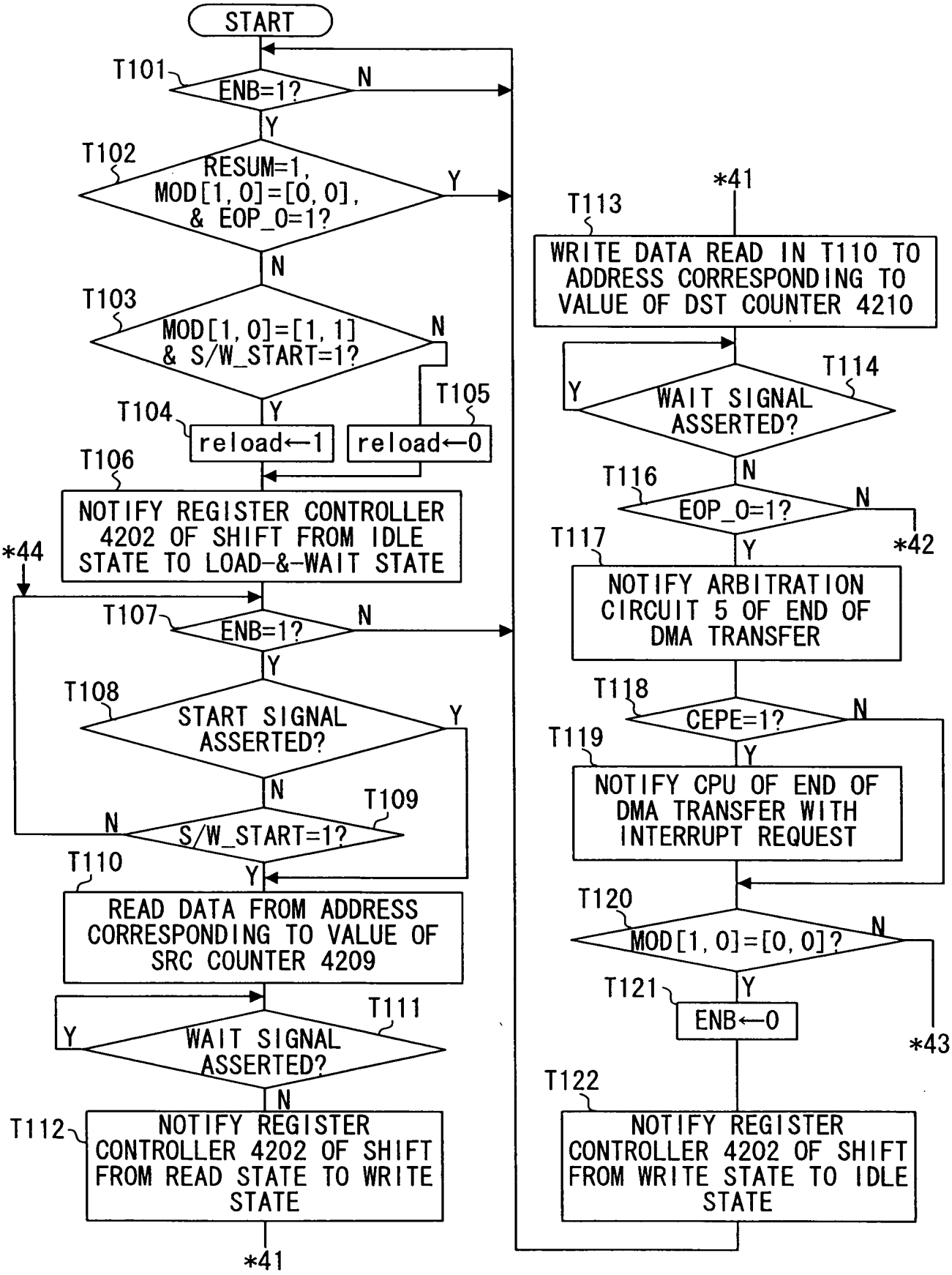


FIG.24

ADDRESS(Hex)	CONTENTS OF DATA
⋮	⋮
20000000-20000003	START ADDRESS(20007774) IN RAM 4400 WHERE INFORMATION NEEDED FOR 2ND DMA TRANSFER SESSION IS STORED
20000004-20000007	INFORMATION INDICATING START ADDRESS OF SOURCE IN 1ST DMA TRANSFER SESSION
20000008-2000000B	INFORMATION INDICATING START ADDRESS OF DESTINATION IN 1ST DMA TRANSFER SESSION
2000000C-2000000D	INFORMATION INDICATING NUMBER OF CYCLES INVOLVED IN ONE DMA TRANSFER SESSION IN 1ST DMA TRANSFER SESSION
2000000E-2000000F	INFORMATION INDICATING NUMBER OF DMA TRANSFER SESSIONS TO BE EXECUTED IN 1ST DMA TRANSFER SESSION
20000010-20000011	OTHER INFORMATION RELATING TO 1ST DMA TRANSFER SESSION
20000012	CONTROL INFORMATION RELATING TO 1ST DMA TRANSFER SESSION S/W_START = 0 MOD[1,0] = [1,1]
⋮	⋮
20007774-20007777	START ADDRESS(ARBITRARY) IN RAM 4400 WHERE INFORMATION NEEDED FOR 3RD DMA TRANSFER SESSION IS STORED
20007778-2000777B	INFORMATION INDICATING START ADDRESS OF SOURCE IN 2ND DMA TRANSFER SESSION
2000777C-2000777F	INFORMATION INDICATING START ADDRESS OF DESTINATION IN 2ND DMA TRANSFER SESSION
20007780-20007781	INFORMATION INDICATING NUMBER OF CYCLES INVOLVED IN ONE DMA TRANSFER SESSION IN 2ND DMA TRANSFER SESSION
20007782-20007783	INFORMATION INDICATING NUMBER OF DMA TRANSFER SESSIONS TO BE EXECUTED IN 2ND DMA TRANSFER SESSION
20007784-20007785	OTHER INFORMATION RELATING TO 2ND DMA TRANSFER SESSION
200077786	CONTROL INFORMATION RELATING TO 2ND DMA TRANSFER SESSION S/W_START = 0 MOD[1,0] = [1,0]
⋮	⋮

FIG.25


START
T101
ENB=1?
N
Y
T102
RESUM=1, MOD[1,0]=[0,0], & EOP_0=1?
Y
N
T103
MOD[1,0]=[1,1] & S/W_START=1?
N
Y
T104
reload←1
T105
reload←0
T106
NOTIFY REGISTER CONTROLLER 4202 OF SHIFT FROM IDLE STATE TO LOAD-&-WAIT STATE
*44
T107
ENB=1?
N
Y
T108
START SIGNAL ASSERTED?
Y
N
T109
S/W_START=1?
N
Y
T110
READ DATA FROM ADDRESS CORRESPONDING TO VALUE OF SRC COUNTER 4209
T111
WAIT SIGNAL ASSERTED?
Y
N
T112
NOTIFY REGISTER CONTROLLER 4202 OF SHIFT FROM READ STATE TO WRITE STATE
*41
*41
T113
WRITE DATA READ IN T110 TO ADDRESS CORRESPONDING TO VALUE OF DST COUNTER 4210
T114
WAIT SIGNAL ASSERTED?
Y
N
T116
EOP_0=1?
N
*42
Y
T117
NOTIFY ARBITRATION CIRCUIT 5 OF END OF DMA TRANSFER
T118
CEPE=1?
N
Y
T119
NOTIFY CPU OF END OF DMA TRANSFER WITH INTERRUPT REQUEST
T120
MOD[1,0]=[0,0]?
N
Y
T121
ENB←0
*43
T122
NOTIFY REGISTER CONTROLLER 4202 OF SHIFT FROM WRITE STATE TO IDLE STATE

Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
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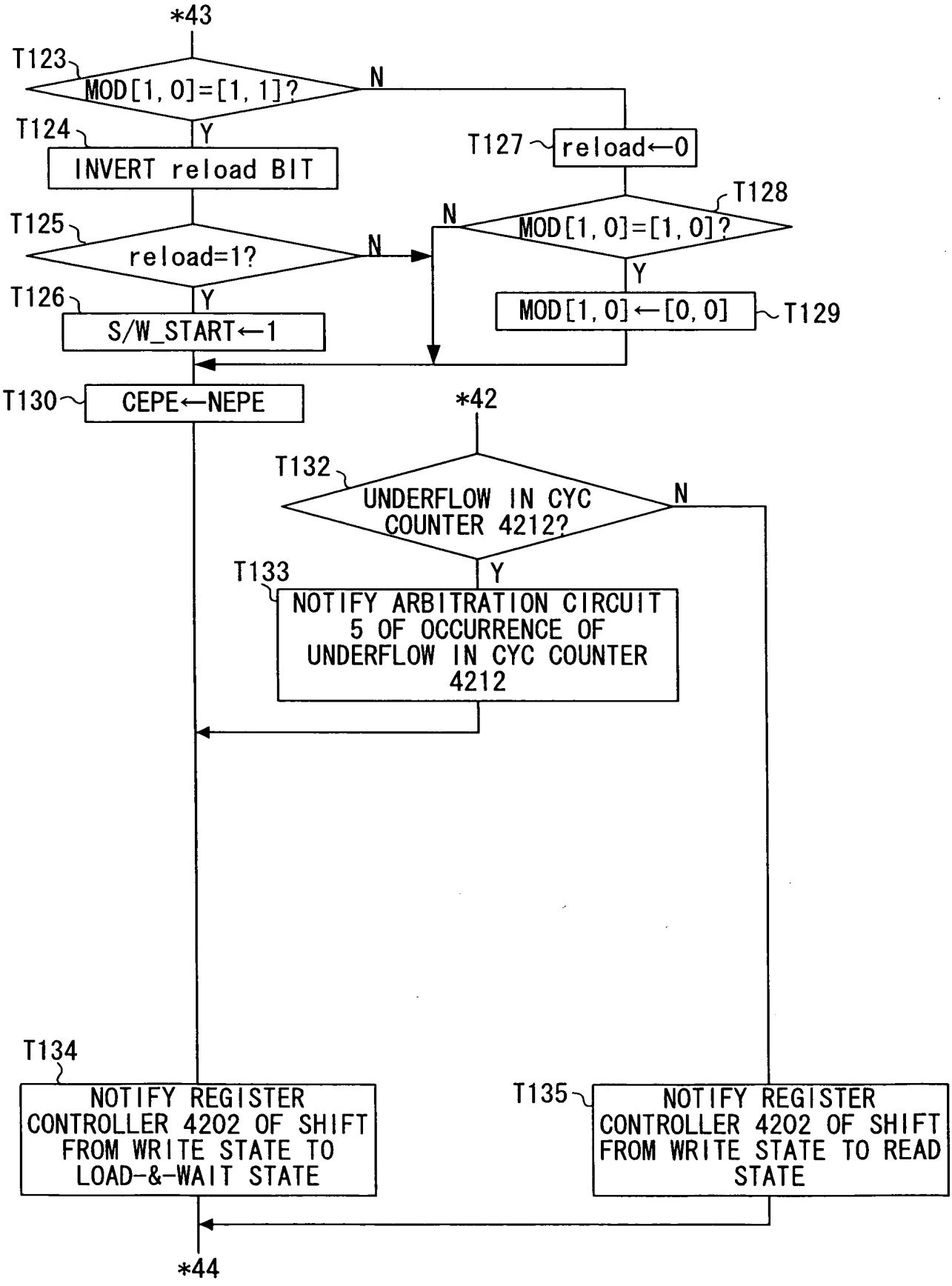
FIG.26



Title: DATA PROCESSING CONTROL APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
Appln. No. : Unknown
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FIG.27

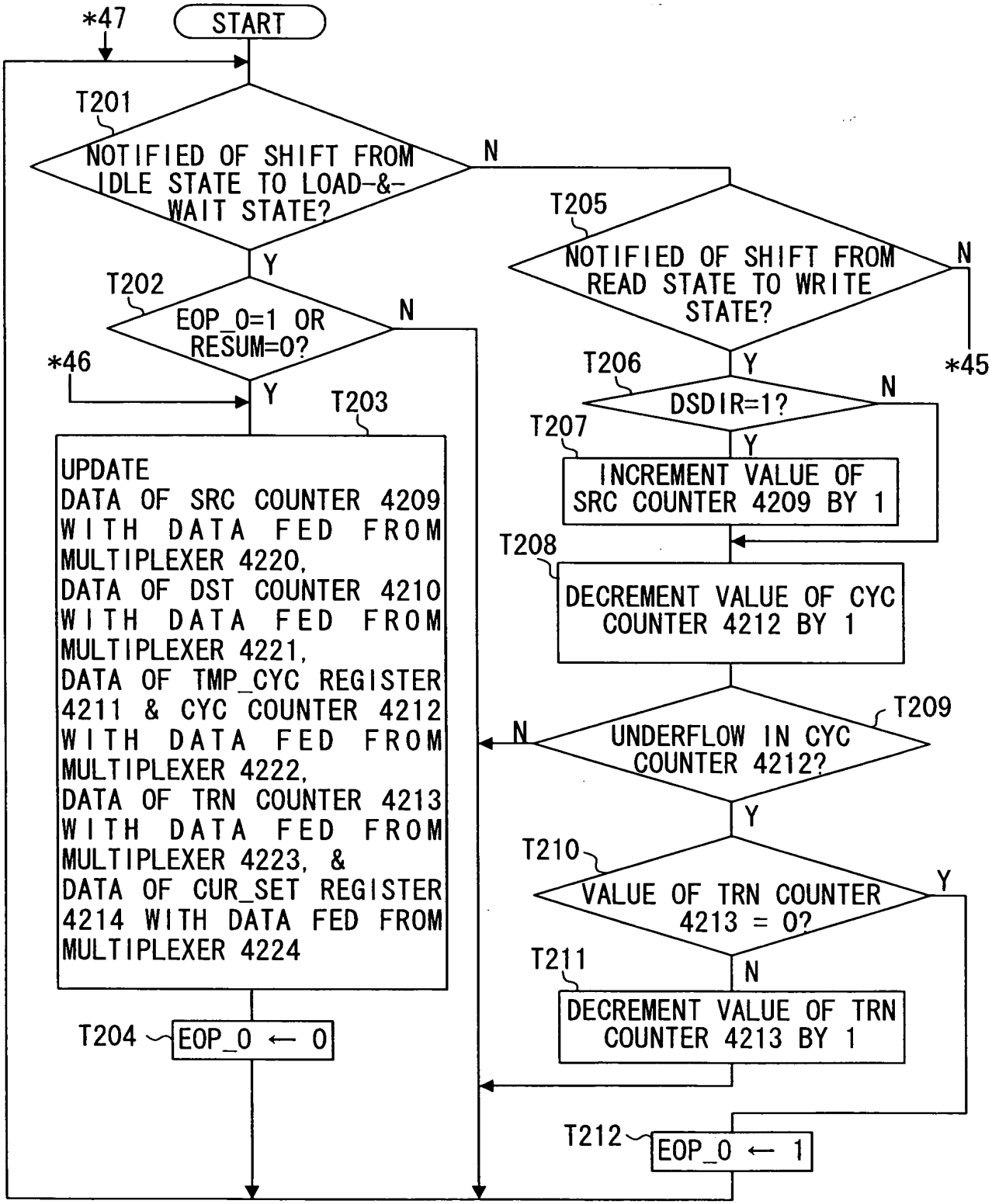
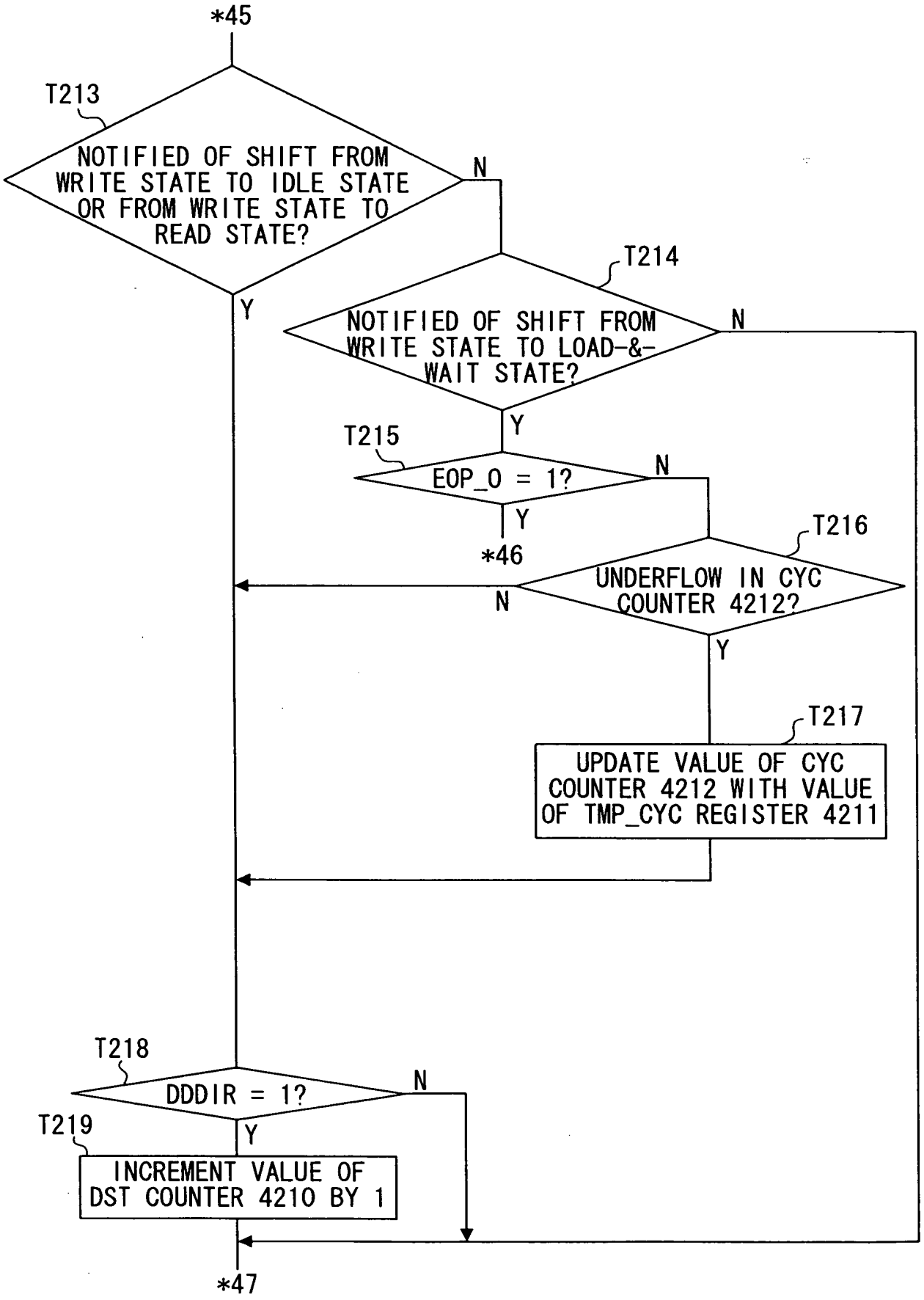


FIG.28


*45
T213
NOTIFIED OF SHIFT FROM WRITE STATE TO IDLE STATE OR FROM WRITE STATE TO READ STATE?
N
Y
T214
NOTIFIED OF SHIFT FROM WRITE STATE TO LOAD-&-WAIT STATE?
N
Y
T215
EOP_0 = 1?
N
Y
*46
T216
UNDERFLOW IN CYC COUNTER 4212?
N
Y
T217
UPDATE VALUE OF CYC COUNTER 4212 WITH VALUE OF TMP_CYC REGISTER 4211
T218
DDDIR = 1?
N
Y
T219
INCREMENT VALUE OF DST COUNTER 4210 BY 1
*47